## SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING BODY BIASING CIRCUIT FOR GENERATING FORWARD WELL BIAS VOLTAGE OF SUITABLE LEVEL BY USING SIMPLE CIRCUITRY

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CROSS REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application Nos. 2002-211536, filed on July 19, 2002 and 2003-019271, filed on January 28, 2003, the entire contents of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

- 1. Field of the Invention
- The present invention relates to a semiconductor integrated circuit device and, more particularly, to a semiconductor integrated circuit device comprising a high-speed, low-voltage operating MISFET.
  - 2. Description of the Related Art

Recently, the widespread use and the increased functionality of portable information apparatuses such as portable telephones and portable PDAs (Personal Digital Assistants) have been driving the need to further increase the operating speed and reduce the power consumption of semiconductor integrated circuit devices constructed from MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors, or more broadly, MISFETs (Metal-Insulator-Semiconductor FETs)).

Conventionally, to reduce the power consumption of CMOS (Complementary MOS) circuits, it has been practiced to reduce the driving power supply voltage. However, as the reduced supply voltage results in a lower operating speed, if the power consumption is to be reduced without compromising the operating speed, the threshold voltage of the MOS transistors has had to be reduced. Reducing the threshold voltage of the MOS transistors leads to faster switching operation of the

MOS circuit, but this in turn results in an increase in subthreshold leakage current, and hence an increase in power consumption.

In view of this, a technique that applies a forward bias voltage as a well voltage (body voltage or back-gate voltage) to a MOS transistor has been attracting attention in recent years. However, application of a forward bias voltage to the well (body) involves other problems such as an increase in chip area due to the addition of a bias voltage generating circuit. There is therefore a need to provide a semiconductor integrated circuit device having a body biasing circuit that can generate a forward body (well) bias voltage of a suitable level by using simple circuitry.

The prior art and its associated problem will be described in detail later with reference to relevant drawings.

## SUMMARY OF THE INVENTION

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An object of the present invention is to provide a semiconductor integrated circuit device having a body biasing circuit that can generate a forward body (well) bias voltage of a suitable level by using simple circuitry.

According to the present invention, there is provided a semiconductor integrated circuit device comprising a MISFET, having a source electrode and a drain electrode of a first conductivity type and a gate electrode, formed in a well of a second conductivity type; and a body biasing circuit that generates a voltage in the well by passing a prescribed current in a forward direction into a diode formed from the well and the source electrode of the MISFET.

The semiconductor integrated circuit device may comprise a plurality of circuit blocks; and the body biasing circuit may be provided for each of the circuit blocks. The semiconductor integrated circuit device may further comprise a power control unit which controls the

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The current source may comprise a current-source fifth MISFET having a different polarity from the MISFET, and whose gate electrode is supplied with a control signal and whose source electrode is connected to the first power supply line; and a current-source sixth MISFET having the same polarity as the MISFET, and whose gate electrode is supplied with the control signal and whose source electrode is connected to the contact region and whose drain electrode is connected to a second power supply line.

Further, according to the present invention, there is also provided a semiconductor integrated circuit device comprising a first MISFET of a first polarity, having a source electrode and a drain electrode of a first conductivity type and a gate electrode, formed in a first well of a second conductivity type; a second MISFET of a second polarity, having a source electrode and drain electrode of the second conductivity type and a gate electrode, formed in a second well of the first conductivity type; a first body biasing circuit that generates a voltage in the first well by passing a prescribed current in a forward direction into a diode formed from the first well and the source electrode of the first MISFET; and a second body biasing circuit that generates a voltage in the second well by passing a prescribed current in a forward direction into a diode formed from the second well and the source electrode of

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polarity as the first MISFET, and whose gate electrode is supplied with an inverted version of the first control signal and whose source electrode is connected to the contact region of the first well and whose drain electrode is connected to the second power supply line; and the second current source may further comprise a second-current-source fourth MISFET having the same polarity as the second MISFET, and whose gate electrode is supplied with an inverted version of the second control signal and whose source electrode is connected to the contact region of the second well and whose drain electrode is connected to the first power supply line. The first current source may comprise a first-currentsource fifth MISFET having a different polarity from the first MISFET, and whose gate electrode is supplied with a first control signal and whose source electrode is connected to the first power supply line; and a firstcurrent-source sixth MISFET having the same polarity as the first MISFET, and whose gate electrode is supplied with the first control signal and whose source electrode is connected to the contact region of the first well and whose drain electrode is connected to the second power supply line, and the second current source may comprise a second-current-source fifth MISFET having a different polarity from the second MISFET, and whose gate electrode is supplied with a second control signal and whose source electrode is connected to the second power supply line; and a second-current-source sixth MISFET having the same polarity as the second MISFET, and whose gate electrode is supplied with the second control signal and whose source electrode is connected to the contact region of the second well and whose drain electrode is connected to the first power supply line. An operation delay may be made constant against temperature changes by operating the semiconductor integrated circuit device with a low voltage at which the semiconductor integrated circuit device exhibits the characteristic that a leakage current

increases and the delay decreases with increasing temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description of the preferred embodiments as set forth below with reference to the accompanying drawings, wherein:

Figure 1 is a circuit diagram showing one example of a prior art semiconductor integrated circuit device;

Figure 2 is a circuit diagram showing another example of the prior art semiconductor integrated circuit device:

Figure 3 is a circuit diagram showing the basic functional configuration of a semiconductor integrated circuit device according to the present invention;

Figure 4 is a cross-sectional view for explaining the basic functional configuration of the semiconductor integrated circuit device according to the present invention;

Figure 5 is a diagram showing diode characteristics for explaining the principle of the semiconductor integrated circuit device according to the present invention;

Figure 6 is a circuit diagram conceptually showing one embodiment of the semiconductor integrated circuit device according to the present invention;

Figure 7 is a circuit diagram showing one configuration example of the semiconductor integrated circuit device shown in Figure 6;

Figure 8 is a circuit diagram showing another configuration example of the semiconductor integrated circuit device shown in Figure 6;

Figure 9 is a diagram showing one example of the layout pattern of an inverter section in the semiconductor integrated circuit device according to the present invention;

Figure 10 is a diagram schematically showing one

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Figure 11 is a diagram schematically showing a
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                                                                               device shown in Figure 10;
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                                                                       the one shown in Figure 9;
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                                                               device shown in Figure 12;
                                                                        Figure 14 is a diagram schematically showing another
                                                          modified example of the semiconductor integrated circuit
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                                                        device shown in Figure 12;
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device to which the present invention
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                                                is applied;
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Figure 16 is a diagram schematically showing a cross
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              is applied;
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Figures 20A and 20B are diagrams for explaining the
        temperature dependence of transistor delay time;
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Figure 21 is a diagram (part 1) showing measurement results for explaining the operation of the semiconductor integrated circuit device according to the present invention;

Figures 22A and 22B are diagrams (part 2) showing measurement results for explaining the operation of the semiconductor integrated circuit device according to the present invention;

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Figure 23 is a diagram (part 3) showing measurement results for explaining the operation of the semiconductor integrated circuit device according to the present invention; and

Figure 24 is a diagram (part 4) showing measurement results for explaining the operation of the semiconductor integrated circuit device according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before proceeding to the detailed description of the semiconductor integrated circuit device according to the present invention, the prior art semiconductor integrated circuit device and its associated problem will be described first, with reference to the drawings.

For high-speed and low-power operation of CMOS circuits, a technique that applies a forward bias voltage to the body (well) of a MOS transistor has been attracting attention in recent years.

Specifically, in the prior art there is proposed a semiconductor integrated circuit device (CMOS chip) that achieves both high-speed operation and low power consumption by applying a forward body bias FBB during active operation and a zero body bias ZBB in standby mode (for example, refer to S. Narendra et al., "1.1V 1GHz Communications Router with On-Chip Body Bias 150nm CMOS," ISSCC 2002/SESSION 16/HIGH SPEED I/O 16.4, pp. 270, 271, 466: February 5, 2002).

In the prior art, there is also proposed a semiconductor integrated circuit device in which

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                                                                                                                                                                                                                                                                                                      Figure 1 is a circuit diagram showing one example of
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                                            Voltage Vaq is, Tor example, Voltage Vbp is Vdd-0.45V (for example, 0.55 V).
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                           circuit device shown in Figure 1, the forward body bias
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voltage Vbp of Vdd-0.45V, for example, is applied to the n-well of the pMOS transistor 201 during operation, and a zero body bias voltage is applied to it (application of the body bias voltage is stopped) in the standby mode, thereby achieving both high-speed operation, due to the reduced threshold voltage (application of the forward body bias voltage) during operation, and reduced power consumption in the standby mode. The impedance device 203 is provided to prevent an excessive current from flowing in the event of a temperature rise, etc.

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Figure 2 is a circuit diagram showing another example of the prior art semiconductor integrated circuit device. In Figure 2, reference numeral 300 is an inverter section, 301 is a pMOS transistor, 302 is an nMOS transistor, 303 and 304 are current sources, and 305 and 306 are bias voltage generating circuits. In Figure 2, reference character Vbn designates an nMOS transistor body bias voltage (bias voltage to the p-channel body (p-channel well region) of the nMOS transistor).

As shown in Figure 2, in the other example of the prior art semiconductor integrated circuit device, the body bias voltage Vbp (output voltage of the bias voltage generating circuit 305) is applied to the n-channel well region (n-well: back gate) of the pMOS transistor 301 via the current source 303, and the body bias voltage Vbn (output voltage of the bias voltage generating circuit 306) is applied to the p-channel well region (p-well: back gate) of the nMOS transistor 302 via the current source 304. Here, the pMOS transistor body bias voltage Vbp is a fixed voltage lower than the high potential supply voltage Vdd by a prescribed voltage, while the nMOS transistor body bias voltage Vbn is a fixed voltage higher than the low potential supply voltage Vss by a prescribed voltage.

More specifically, in the semiconductor integrated circuit device shown in Figure 2, the forward body bias voltages to be applied to the MOS transistors, for

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                                                               Configuration in which the prior art proposes the conductor integrated
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                                           requiring a certain amount of circuitry has to be example. about 0.5 VI. Furthermore age to be
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                                   aegree of margin, the body blas voltage is reducing the transistor threshold
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                          Semiconductor integrated circuit device according to the
                        present invention will be described.
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                                 Figure 3 is a circuit diagram showing the basic
                    functional sis a circuit alagram showing the basic from the present integrated
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               Figure 4 is a cross-sectional view for explaining the
             basic functional configuration of the semiconductor
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           integrated circuit device according to the present
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       the part of the nMOS transistor (2) shown in Figure 4.
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The inverter (CMOS inverter) constructed with the pMOS transistor 1 and nMOS transistor 2 will be described in detail later in conjunction with Figure 4.

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In Figures 3 and 4, reference numeral 2 is the nMOS transistor, 4 is a current source, and 21 is a diode (parasitic diode). In Figure 4, reference numeral 2a is a conducting electrode, 2b is an insulating film, 20 is a p-channel semiconductor substrate (p-channel well), 20a is a  $p^+$  diffusion region, and 20b and 20c are  $p^+$  diffusion regions.

As shown in Figures 3 and 4, the nMOS transistor 2 is formed in the p-channel well (p-well) 20, and comprises the n<sup>+</sup> diffusion region (source electrode S) 20b, the n<sup>+</sup> diffusion region (drain electrode D) 20c, and the conducting electrode (gate electrode G) 2a separated by the insulating film 2b. In a conventional pMOS transistor (reverse body biased transistor), a low potential supply voltage Vss would be applied to the p-well 20 (the back gate of the nMOS transistor 2) via the p<sup>+</sup> diffusion region (contact region) 20a, but in the present invention, a high potential supply voltage Vdd is applied to the contact region (p<sup>+</sup> diffusion region) 20a via the current source 4. The diode 21 shown in Figure 3 is formed between the p-well 20 and the source electrode (S) 20b.

According to the present invention, the body bias voltage Vbn is generated with the output current (constant current) Ibn of the current source 4 flowing in a forward direction into the diode 21 formed from the p-well 20 and the source electrode S (n\* diffusion region 20b). Here, the current Ibn is set to a negligibly small value compared with the current, including the switching current, that flows through the entire circuit (for example, to a value equal to or smaller than one tenth of the current flowing through the entire circuit).

Figure 5 is a diagram showing diode characteristics for explaining the principle of the semiconductor

integrated circuit device according to the present invention.

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As shown in Figure 5, the diode (21) exhibits different current-voltage characteristics at different temperatures (for example, at 75°C, 25°C, and -25°C). In the present invention, as the constant output current Ibn of the current source 4 flows into the diode 21, the largest possible body bias voltage at each temperature can be applied to the p-well 20.

That is, in the prior art, in the case of the forward body bias voltage Vbn applied to the p-well 20, as the setting is made by considering, for example, the upper limit temperature defined in the specification of the semiconductor integrated circuit device (for example, 75°C by allowing a certain margin), it has not been possible to reduce the threshold voltage of the transistor (pMOS transistor 2) as much as possible by increasing the forward body bias voltage (Vbn), and as a result, it has been difficult to maximize the operating speed of the circuit.

On the other hand, according to the semiconductor integrated circuit device of the present invention, the operating speed of the circuit can be maximized according to the operating temperature. Furthermore, according to the semiconductor integrated circuit device of the present invention, as the output of the current source is applied to the well (body) by using the contact region directly, and the body bias voltage is generated by using the diode formed from the well and the source electrode (diffusion region), the circuit configuration is simple and the chip area can be reduced. Moreover, according to the semiconductor integrated circuit device of the present invention, as the current for generating the forward body bias voltage is regulated by the current source, the power consumption (the current flowing through the circuit) can be controlled independently of temperature changes, etc.

Embodiments of the semiconductor integrated circuit device according to the present invention will be described in detail below with reference to the accompanying drawings.

Figure 6 is a circuit diagram conceptually showing one embodiment of the semiconductor integrated circuit device according to the present invention; a CMOS inverter section is shown here. In Figure 6, reference numeral 1 is a pMOS transistor, 2 is an nMOS transistor, 11, 12, 21, and 22 are diodes (parasitic diodes), and 3 and 4 are current sources.

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As shown in Figure 6 and also in Figure 4 previously given, the nMOS transistor 2 is formed in the p-well 20, and comprises the source electrode S (n<sup>+</sup> diffusion region 20b), the drain electrode D (n<sup>+</sup> diffusion region 20c), and the gate electrode G (conducting electrode 2a) separated by the insulating film 2b. Likewise, the pMOS transistor 2 is formed in the n-channel well (n-well) 10, and comprises the source electrode S (p<sup>+</sup> diffusion region) 10b, the drain electrode D (p<sup>+</sup> diffusion region) 10c, and the gate electrode G (conducting electrode) 1a separated by the insulating film 1b.

In the nMOS transistor 2, the current source 4 coupled to the high potential supply voltage Vdd is connected to the contact region (p<sup>+</sup> diffusion region) 20a, and flows the forward current Ibn into the diode 21 formed from the p-well 20 and the source electrode S (n\* diffusion region 20b). With the current Ibn flowing through the diode 21, a prescribed forward body bias voltage Vbn is generated in the p-well 20. Here, as earlier described with reference to Figure 5, the body bias voltage Vbn changes to an optimum level according to the operating temperature; that is, when the operating temperature is high (for example, 75°C), the body bias voltage Vbn decreases and the transistor threshold voltage is set higher, while when the operating temperature is low (for example, -25°C), the body bias

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supply line (Vdd) to the low potential power supply line (Vss: the source electrode of the nMOS transistor 2) via the pMOS transistor 44, the p-well 20 (Vbn), and the diode 21. Here, when the control signal Cbn is at the high level "H", the nMOS transistor 40 is OFF because the control signal Cbn whose level is inverted to the low level "L" by the inverter 41 is applied to the gate of the nMOS transistor 40.

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On the other hand, when the control signal Cbn is at the low level "L", the nMOS transistor 42 is OFF and the nMOS transistor 40 is ON, so that the low potential supply voltage Vss is applied to the back gate (p-well 20) of the nMOS transistor 2.

Likewise, the current source 3 comprises an inverter 31, pMOS transistors 30 and 32, and nMOS transistors 33 15 and 34. When a control signal Cbp is at a low level "L", the pMOS transistor 32 is ON, current flows to the nMOS transistor 33, and the current Ibp flows through the nMOS transistor 34 connected to the nMOS transistor 33 in a current-mirror configuration. That is, when the control 20 signal Cbp is at the low level "L", the current Ibp flows from the high potential power supply line (Vdd: the source electrode of the pMOS transistor 1) to the low potential power supply line (Vss) via the diode 11, the n-well 10 (Vbp), and the nMOS transistor 34. 25 Here, when the control signal Cbp is at the low level "L", the pMOS transistor 30 is OFF because the control signal Cbp whose level is inverted to the high level "H" by the inverter 31 is applied to the gate of the pMOS transistor 30.

On the other hand, when the control signal Cbp is at the high level "H", the pMOS transistor 32 is OFF and the pMOS transistor 30 is ON, so that the high potential supply voltage Vdd is applied to the back gate (n-well 10) of the pMOS transistor 1.

Figure 8 is a circuit diagram showing another configuration example of the semiconductor integrated circuit device shown in Figure 6; another example of the

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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             (current sources 3 and 4) shown in Figure 8 is somewhat in Figure 7 in the circuit shown in Figure 3 and 4. the circuit shown in Figure 8 is somewhat in Figure 7 in Figure 8 is somewhat in Figure 9 is Figure 7 in Figure 8 is somewhat in Figure 9 
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Figure 1. In the current sources levels of the control

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Sources 3 and 4 snown in the circuits who are who is a source who are the product of 
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Controlled based on the Here, the control signal. Further as a 1-bit signal.
                                    and CDP, respectively. Here, the control signals further, for constructed as a 1-bit signal. Further, for constructed as a 1-bit signal.
                                                    Cop can each be constructed as a 1-bit signal. Further, for the body biasing circuit hlock or each functional the body for each circuit hlock or each functional
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                                                                                      example, for each circuit block or each functional can each circuit block or each the circuit up later, without taking up circuit; as will be described later, without taking up circuit; as will be aimole circuit.
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                                                                                                                                  much chip area. It will also be appreciated that the shown circuit configuration are now he modified in various wave.
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                                                                                                                                                                                    rigure y is a glagram snowing one example in the inverter section in the layout pattern of the inverter section.
                                                                                                                                                                                                                                     present invention, and Figure 10 is a semiconductor of invention, and Figure 20 is a semiconductor of invention, and Figure 10 is a semiconductor of invention o
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                                                                                                                                                                                                                semiconductor integrated circuit device according present invention;
                                                                                                                                                                                                                                                  schematically showing one example of a semiconductor inverter a plurality of inverter a plurality of inverter a plurality of inverter integrated circuit device having a plurality in Figure 9.
                                                                                                                                                                                                                                                                integrated circuit device naving a plurality or inverted to the one shown in Figure 9.
                                                                                                                                                                                                                                                                                                                                                              Lons each in Figure 4 and Figures 6 to 9, the roots and Figure 4 and Figure 30, 100 to 50 
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Notage Vbn is applied to the powell transistor?

Notage vbn is region 2021 of the number transistor?
                                                                                                                                                                                                                                                                                                               Voltage von 15 applied to the p-well 20 (contact region is applied to the nMOS transistor in Iront of the nMOS annied to the n-well in Iront pt diffusion region von is annied to the n-well in Iront pt he hims voltage von the new von t
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                                                                                                                                                                                                                                                                                                                                 P. diffusion region 20a) of the nMOS transistor 2, and the nMOS transistor 
                                                                                                                                                                                                                                                                                                                                                the bias voltage vpp 1s applied to the pMOS transistor the bias voltage vpp 1s applied to the pMOS are connected to the the bias voltage vpp 1s and vpn are connected to the region; nt diffusion region and vpn are connected to the region; nt are trained to the pMOS transistor.
                                                                                                                                                                                                                                                                                                                                                              region; n diffusion region lual of the pwus translator the viring and vbp are connected to wiring these these rirguit line for example via metal wiring these hiseing circuit
                                                                                                                                                                                                                                                                                                                                                                           1: these blas voltages von and vop are connected to the first body blasing M12 and M11 M14 respectively. In the first
                                                                                                                                                                                                                                                                                                                                                                                             body biasing circuit 110, for example, via metal wiring in the first N14, respectively, in lines (via N14, respectively, in the lines (via N14, respectively, in lines
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Refer the high potential power supply lines (vec) are

Refer refertial remarkable for the first remarkable for the 
                                                                                                                                                                                                                                                                                                                                                                                                                               Layer. Here, the night power supply lines (Vss) are and the low potential power supply for evample and the low potential power for evample for evample and the low potential power for evample for eva
                                                                                                                                                                                                                                                                                                                                                                                                                                               and the low potential power supply for example, by respectively connected in common, and M22 in the respectively maral wiring lines M21 and M22.
                                                                                                                                                                                                                                                                                                                                                                                                                                                              respective metal wiring lines M21 and M22 in the second respective metal wiring lines M21 and M22 in the second respective metal wiring lines M21 and M22 in the second wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 in the second metal wiring lines M21 and M22 and M2
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further, as shown in Figures (CMOS patterns) 120,

a plurality of inverter sections or ison, each income and arrange in the plurality of the p
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          a plurality of inverter exclusive on (EOR) sections block a plurality of 121, and exclusive on each circuit block nAND sections are orderly arranged in each circuit block arranged in eac
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               NAND sections are orderly and who from the hody biasin for example; woltages (who and the bias voltages)
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            and the plas voltages (vpn and vpp) trom the pody 120, are supplied to the respective gates 120, circuit 122 off
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Figure 11 is a diagram schematically showing a
                   Figure 11 is a diagram schematically showing a circuit semiconductor integrated circuit semiconduct
                                                                                                                           snown in Figure 10. comparison between Figures 11

As is apparent from a comparison between Figures 11
                                                                As is apparent from a comparison between Figures 11

As is apparent from example, ..., to the respective and 10, in the modified who?
                                                                               and 10, what worter sections 120, wand sections 122, while work of the modified example, which is to the respective when which is the modified example, which is to the respective when which is to the respective when which is the modified example, which is to the respective which we would not be a section which we would not be a section which we would not be a section when we will not be a section with the section when we will not be a section with the section when we will not be a section when we will not be a section with the section when we will not be a section with the section when we will not be a section with the section will not be a
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                                          device shown in Figure 10.
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                                                                                                                                                                          Voltage pair Vbn, in the modified example shown in rigure in the modified example shown. Vbnl: Vbnl: vbnl of bias voltage pairs vbnl.
                                                                                                                                                                                         circuit 110 but, in the modified example snown in figure pairs vbnl, vbpl; are out of bias voltage pairs the hody hiasing the bias voltage pairs the hody hiasing hiasing hiasing hiasing hiasing
                                                                                                                                                                                                     Vbpl; vbn2, vbpl; vbpl; vbpl; vbpl; vbpl; vbpl; vbpl; vbpl; voltage pairs vbnl, biasing the body biasing the body biasing the output from the body he are output from the body he will be appropriate control can he vbpl; vbp
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                                                                                                                                                                                                                         VDP2: VDD3: ... are output from the pour be circuit 110: so that more precise control can be
                                                                                                                                                                                                                                                                                                                              aved. 12 is a diagram schematically showing another rigure to comin and community across the second community acro
                                                                                                                                                                                                                                                                     example of the semiconductor inverter sections each identical example of the semiconductor inverter sections and the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the semiconductor inverter sections are sections as a section of the section
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                                                                                                                                                                                                                                                                                                                                             semiconductor integrated circuit device snown in Figure 14 is a diagram schematically showing and Figure 14 is a common of the c
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Clrcult devices integrated circuit devices are controlled by noting the semiconductor bias voltages are controlled by noting the semiconductor bias voltages.
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                                                                                                                                                                                                                                                                                                                                                                                                           semiconductor integrated circuit devices snown in Figures the bias voltages are controlled by noting the lias voltages are and nunce transistors and nunce transistors and nunce transistors are arrangement of nunce transistors.
                                                                                                                                                                                                                                                                                                                                                                                                                            to 14, the plas voltages are controlled by noting transistors and nMOS transistors and nMOS transistors are controlled by noting transistors.
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transistors and nMOS transistors

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arrayed in the Town arrangement of the transistors
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                      CMOS circuit, the transistors of the transistors of
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      type) are usually arranged in the row direction and, the transistors of 14, the transistors circuits adjacent cMOS circuits two adjacent cMOS circuits two adjacent two adjacent two adjacent two except in the conductivity type
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the same conductivity type in two be adjacent each other amanner as to be adjacent each other two omns circuits.
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are formed in such a manner as to be two interrated in the column direction between the two interrated in the column direction the semiconductor interrated.
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circuit device comprising CMOS circuits, the well region of the same conductivity type (n-well or p-well) is shared between two CMOS circuits adjacent in the column direction, and the same bias voltage is applied to the well region of this same conductivity type.

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The semiconductor integrated circuit device shown in Figure 12 is similar to the semiconductor integrated circuit devices shown in Figures 10 and 11, but is drawn from a different viewpoint; that is, one body biasing circuit 110 is provided for a standard cell block 400 that forms the semiconductor integrated circuit device, and the bias voltages Vbp and Vbn are applied from the body biasing circuit 110 to the p-well regions and the n-well regions, respectively, in the standard cell block 400.

In the semiconductor integrated circuit device shown in Figure 13, the standard cell block 400 is divided into a plurality of (two) groups 401 and 402, and body biasing circuits 411, 412 and 421, 422 are provided for the respective cell groups 401 and 402. Here, in the semiconductor integrated circuit device shown in Figure 13, the body biasing circuits 411 and 421 for the p-well regions and the body biasing circuits 412 and 422 for the n-well regions are provided for the respective cell groups 401 and 402, and the body bias voltages Vbpa, Vbpb and Vbna, Vbnb are controlled by the respective control signals CSpa, CSpb and CSna, CSnb supplied from the control circuit 410.

In the semiconductor integrated circuit device shown in Figure 14, transistors of different conductivity types are formed adjacent to each other; in this case, the body bias voltage for each adjacent region can be controlled independently of the other. Body biasing circuits 430-1 to 430-n are provided one for each row of the standard cell block 400, and the body bias voltages Vbp-1, Vbn-1 to Vbp-n, Vbn-n are controlled by the respective control signals CS-1 to CS-n supplied from the control circuit

410.

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In this way, the arrangement of the standard cell block and the body biasing circuits (and the control circuit) can be modified, variously, as needed. For the body biasing circuit configuration, the circuit configuration shown in Figure 7 or 8 can be applied in its entirety.

Figure 15 is a block diagram showing the entire configuration of one example of the semiconductor integrated circuit device to which the present invention is applied. In Figure 15, reference numeral 100 is the semiconductor integrated circuit device (one-chip IC); 101 to 103 are circuit blocks, that is, 101 is a CPU (Central Processing Unit), 102 is a DSP (Digital Signal Processor), and 103 is other circuit block such as a logic circuit, memory circuit, etc.; 104 is a bus; 105 is a power control unit; and 111 to 113 are body biasing circuits.

As shown in Figure 15, the respective circuit blocks 101 to 103 are interconnected via the bus 104, and transfer various data and signals among them. circuit blocks 101 to 103 are respectively provided with the body biasing circuits 111 to 113 which are controlled by control signals from the power control unit 105, and the body biasing circuit only for the necessary circuit block is activated according to the operating state of the semiconductor integrated circuit device 100. the body biasing circuits 111 to 113 can each be constructed employing the circuit configuration described with reference to Figure 7, and can be controlled according to the level, i.e., the high level "H" or the low level "L", of the control signal ("1" or "0" of the one-bit control signal) supplied from the power control unit 105.

35 That is, the body biasing circuits 111 to 113, small in size and simple in configuration, are provided for the respective circuit blocks 101 to 103 and, by controlling

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the operation of the body biasing circuits 111 to the the operation of the body phiasing circuits according to the the reenentive one-hit control signals.
                   the operation of the nower consumntion can be further the respective the nower consumntion can be formal to the control signals according to the nower consumntion can be further the respective.
                                 tne respective one-plt control signals according to the the power consumption can be further than the power can be further 
                                                                                                                                  ged. 16 is a diagram schematically showing a cross rigure to is a diagram schematically showing a cross across a diagram schematically showing a cross across a construction of the constr
                                                                            section of the semiconductor integrated circuit device
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                                                                                                                                  circuit blocks 101 to 103 shown in Figure 15 is circuit blocks
                                                         reduced.
                                                                                                                                                                    constructed, for example, in a triple well structure, and constructed, for example, locks (CPU 101, are electric, the respective circuit income.
                                                                                                                                                                                the respective circuit blocks (CPU 101, DSP 102, and are electrically the respective circuit with this structure, with this structure, logic circuit/memory circuit with this structure, and the logic circuit/memory circuit with this structure, with this structure, and the logic circuit/memory circuit with this structure, with this structure, and the logic circuit/memory circuit with this structure.
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As snown and a body biasing circuit accordance with direction accordance with dir
                                                                                                                                                                                                                                                                                                                                                                                          pplied. in Figure 17, a CPU 101 comprises a map
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register 132, register 133 and a body biasing circuit.
                                                                                                                                                                                                                                                                                                              is applied.
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              CPU 101. Specifically the soft ware module is fetched to the soft ware module is fetch
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          mory or the registers 112 and 113 are connected 112
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          the CPU 101. The registers 112 and 113 are connected to 104.

the data bus from the CPU 101 through the data bus from the cPU are written
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The accordance with this example, bower management
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                                                                                                                                                                       on the one-chip IC 100.
                                                                                                                                                            configuration of a block alagram showing the semiconductor integrated circuit danother example of
                                                                                                                                                                                         Figure 18 is a block diagram showing the
                                                                                                                                                        the semiconductor integrated circuit device to which the diagram shows for
                                                                                                                                                  present invention integrated circuit device to which in the diagram shows, for
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                                                                                                                                              present example, a CPU 1010 (sappled; the alagram shows, for shown
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                                                                                                                                                           As shown in Figure 18, the CPU 1010 comprises a and how,
                                                                                                                              As snown in rigure

hiasing of functional blocks lile to live comprises a

nrovided for the
                                                                                                                           biasing circuits lill to lidl are provided for the
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                                                                                                                        respective functional blocks lillo to lique are province to the first 
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for the memory block body blasing circuit 1111

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                                                                                                    register blocks 1120 and 1130, respectively, and the rowinder
                                                                                               register blocks 1120 and 1130, respectively, and the hody biasing circuit

The body biasing circuit 1141 is provided
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to lile to block lile to block lile to lile to lile body bias voltages (Vbp and Vbn)
                                                                                 in the corresponding the body bias voltages (vbp and visional blocks 1110 to 1140 by and visional blocks 1110 to 1140 by and visional blocks 1110 to 1140 by and visional blocks 1100 by and visional 
                                                                             the respective functional blocks lile to orrens; and orrens; and ordered to the control signals supplied
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                                                                          from the control circuit 1040.
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                                                                                           In this way, the body bias voltages (Vbp and Vbn)
                                                              can be controlled more precisely by performing control hlock (for
                                                          tor each functional block in each circuit block (for north arguments of the control of the contr
                                                    example, the CPU), not by performing control for each

and the non in a the not of the each

tor each
                                                example, the CPU), not by Performing control for each

Figure 15.

Such as the CPU 101 and the DSP 102, as in
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                                              Figure 15.
                                                              Figure 19 is a block diagram schematically showing a anning of the eam; conductor
                                 still another configuration example of the semiconductor of invention
                             integrated configuration example of the semiconquictor of the example of the present invention of the combined
                        is applied; that is, one example of a circuit combined of shown here.
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                    Ls applied; with a gated; that is, one example of a circuit combined in Figure 19. in the semiconductor here.
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integrated circuit device, logic outputs taken between a logic outputs taken between a and control signals can and control signals can and control signals can and control signals can between a logic outputs taken logic outputs taken between a logic outputs taken logic outputs log
                                                                clock signal clk and control signals csA and csB; A (153)

clock signal clk and control signals to a circuit A (163) in a circuit are supplied as circuit A (163) in a circuit respectively; block 150 and a circuit are supplied as circuit are suppl
                                  Integrated circuit device, logic outputs taken bety control signals CSA and control signals to a direction clock signal cuk and control signals to a direction clock signal cuk and control signals to a direction control signals.
                                                                                      respectively are supplied as circuit as circ
                                                                                                               In a circuit block 150 and a circuit B (163) in a circuit the output the output the output the control signal which and the control signal block 160, respectively. Which and the control signal of an AND gate 171 which sign
                                                                                                                                              block 160, respectively. More specifically, the output the signal which ANDs the control avamnia for a
                                                                                                                                                                   signal of an AND gate 171 which and the circuit.

Signal of an AND gate 171 which is supplied, the circuit.

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                                                                                                                                                                                                                                                     plock 150, while the output signal of an AND gate signal of the clock signal csB with the clock signal innut of a flin-flow innut of a flin-flow which ANDs the control signal innut of a flin-flow which and the clock is supplied to the clock is su
                                                                                                                                                                                                                                                                               which ANDS the control signal cock input of a flip-flop 150 is control signal clock input of a flip-flop 150 is clock input of a flip-flop 150
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The effect of this circuit.

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When there is no need to only can AC power be reduced by the the respective flip.

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flops 152 and 162 has an nower can also be reduced by

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ing circuits 151 and 161.

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woltage CMOS specifically, in K. kanda et al.,
increases.
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   biasing circuits 151 and 161.
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Current in Sub-1-V CMOS 10 or Current in Sub-1-V CMOS 10 or Current curren
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With a voltage lower for a continuous and the state of t
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       with a voltage lower than the with 0.5 V, a voltage with 0.5 V, a voltage coefficient) point (for example, with coefficient)
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lower than 0.7 V), the delay decreases as the temperature increases, unlike the case where it is operated with a high supply voltage (for example, 3.3 V).

Figures 20A and 20B are diagrams for explaining the temperature dependence of the transistor delay time:
Figure 20A shows the relationship between the current Ib flowing through a diode and the generated voltage Vf, and Figure 20B conceptually shows the case where the present invention is applied to a CMOS circuit operating with a low voltage (for example, a voltage lower than 0.7 V).

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In the semiconductor integrated circuit device according to the present invention, as shown in Figure 20A for example (or as described with reference to Figure 5), when the current Ib flowing through the diode (that is, the body bias current Ibn flowing through the diode 21 in Figures 6 and 7) is held constant, the value of the generated voltage Vf (the body bias voltage Vbn) decreases as the temperature rises.

As a result, the transistor threshold voltage Vth increases with increasing temperature, as shown in Figure 20B. Accordingly, when the present invention is applied to a CMOS circuit operating with a low voltage, for example, a voltage lower than 0.7 V, the characteristic of the low-voltage operating CMOS circuit that the delay decreases with increasing temperature, as illustrated in the above-cited paper ("Design Impact of Positive Temperature Dependence on Drain Current in Sub-1-V CMOS VLSI"), is cancelled (qualitatively offset) and the delay of the circuit operating speed can be maintained constant against temperature changes.

Figures 21 to 24 are diagrams showing measurement results for explaining the operation of the semiconductor integrated circuit device according to the present invention.

Figure 21 is a diagram plotting the delay time as a function of the supply voltage (Vdd), measured when a 32-bit ALU (Arithmetic and Logic Unit) is operated at 27°C,

for the case where the body biasing circuit is operated (ALU01/ACT) in comparison with the case where the body biasing circuit is stopped (ALU01/STB).

As can be seen from Figure 21, over the entire range of the supply voltage Vdd from 0.40 V to 1.00 V, the delay time can be reduced more effectively when the body biasing circuit is operated than when it is not operated.

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Figures 22A and 22B are diagrams showing the delay time measured by operating the 32-bit ALU at various supply voltages Vdd (Vdd = 0.35, 0.40, 0.50, 0.60, 0.70, 0.80, 0.90, and 1.00 V) while varying the temperature T: Figure 22A shows the case where the body biasing circuit is operated (ALU01/Active), and Figure 22B shows the case where the body biasing circuit is stopped (ALU01/Standby).

As can be seen from a comparison between Figures 22A and 22B, the delay time can be reduced more effectively when the body biasing circuit is operated than when it is not operated, regardless of the supply voltage Vdd or the temperature TEMP; in particular, it is shown that the lower the supply voltage Vdd and the lower the operating temperature TEMP, the more pronounced the effect of the delay time reduction.

Figure 23 shows the speedup rate (percentage) SP achieved when the 32-bit ALU is operated at various temperatures ( $70^{\circ}$ C,  $27^{\circ}$ C, and  $-25^{\circ}$ C) while varying the supply voltage Vdd. Here the speedup rate SP is obtained as SP = (1-ACT/STB) × 100[%]. Here, ACT is the delay time when the body biasing circuit is operated, and STB is the delay time when the body biasing circuit is not operated.

Figure 24 is a diagram simulating the generation of the body bias voltage based on the control signal Cbp and the resulting change of the n-well voltage level in the n-well (10) of the pMOS transistor.

As can be seen from Figure 24, when the control signal Cbp changes at timing P0 (from the low level "L"

to the high level "H": refer to Figure 7), for example, the voltage level of the n-well 10 shown in Figure 4 immediately drops and settles at timing P1 to the prescribed voltage (Vbn) which means the application of the forward bias voltage. When the control signal Cbp changes from the high level "H" to the low level "L", since the nMOS transistor 42 is turned off and the nMOS transistor 40 is turned on, as earlier described with reference to Figure 7, the voltage level of the n-well 10 immediately rises back to its original level (Vss). That is, as shown in Figure 7, for example, the body biasing circuit 110 (current source 3) can quickly respond to the change of the control signal Cbp (for example, a 1-bit signal).

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As described in detail above, according to the present invention, a semiconductor integrated circuit device can be provided that has a body biasing circuit that can generate a forward body (well) bias voltage of a suitable level by using simple circuitry.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.